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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/301,284	04/28/1999	SHUICHI TAKAYAMA	NAK1-BG86	5392

7590 07/15/2004

MCDERMOTT, WILL & EMERY
600 13TH STREET N W
WASHINGTON, DC 20005-3096

EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/301,284	TAKAYAMA ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/29/04, supplemental Amendment*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11 and 49-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11 and 49-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the supplemental amendment filed on 4/29/2004 that replaces for the amendment filed on 4/26/08.

In regards to the supplemental amendment filed on 4/29/2004:

Claim 1, and Claims 12-48 are canceled; Claims 2-10, and 49-50 are amended; Claim 51 is new in this action.

Claims 2-11, 49-51 are pending in the application.

Response to Arguments

2. With regards to the argument in replying to the office rejection of Claims 1-11, and 49-50 (Claim 1 is now canceled) under 35 USC 112 first paragraph regarding to limitation "*the number processing target instruction being an operation to be executed by the processor, the number of processing target instructions being any natural number except for a power of 2*", where Applicants stated, "Accordingly, the number of instructions which are available would not be understood by those skill in the art to be an infinitive number, but would be within practice boundary of the art and within the spirit of the disclosed invention" (Remarks: page 11), the rejection to Claims 2-11, 49-50 under this statute is withdrawn. To make clear the position to the previous rejection under this statute of the previous office action is based on a big natural number, not an infinitive number, and at the time of this filling application, the practice boundary of the natural number is very limited due to circuitry timing. Therefore, this rejection withdrawal is based on Applicants' assertion "within practice boundary of the art" as disclosed in the specification at the time of filing the application.

3. Applicants' arguments of claimed rejection over Christie have been fully considered. However the arguments are not persuasive.

Regarding the applicant's argument that Christie does not disclose feature "*the number processing target instruction being an operation to be executed by the processor, the number of processing target instructions being any natural number except for a power of 2*" (Remarks: page 12).

Examiner respectfully responds: a natural integer resulting from substituting into the power of power of 2 would be 1, 2, 4, 8, 16. Christie's teaching relates to RISC instruction set consisting of a 4-bytes procession packet. The claim limitation negates the integer number 4, but circuitry mechanism remains the same, by claiming "*except for a power of 2*". Such limitation does not substantially make the functionality difference between two mechanisms (Christie: four-bytes processing packet; Claimed limitation: not four-bytes processing packet) but intended to exclude the use of such a reference under 35 U.S.C. 103, where Examiner establishes the prima facie as the rejection under 35 U.S.C. 103, given in sections 4-5 below.

In response to applicant's argument (Remarks: page 13) that a rejection must be based on evidence. However, the evidence is in the logical nature of counter structure: Four example, 2 bit counter counts up to four numbers, 3 bit counter counts up to 8 numbers; therefore it would be obvious to disable the logics that form the numbers of power of 2, then the such a counter will perform counting the natural numbers that are *except for a power of 2*". This example is not a speculation, but it is the basis in logic design, known and available to relevant skills; and the example above also accounts for the request evidences as requested by Applicants (Remarks pages 13, lines10-11).

in response to the argument there is no suggestion, teaching or motivation (Remarks page 13), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2-11, 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Christie et al., US Patent No. 5,559,975.

As per claim 49:

-Regarding claim limitations:

"*A processor for reading instructions from a memory comprising:*

a memory configured to store (see column 7, lines 33-49, queue), *in a position corresponding to a byte boundary* (see column 7, lines 33-49, ROP), *at least one processing packet being made of a natural number of bytes, the processing packet including processing target instructions, each processing target instruction being an operation to be executed by the processor* (see column 18, lines 4-24, least significant four bits), *the number of processing target instructions being any number except for power of 2;*

a first address indicator configured to indicate a storage position of the processing packet in the memory (see column 18, lines 24-38, more significant program counter; see FIG. 9A: PC Latch (31:4) 704); and

a second address indicator configured to indicate a position of a processing target instruction in the processing packet (see column 18, lines 4-23, less program counter; see FIG. 9A: PC Latch (3:0)

706) *by using the same number of positions as the number of processing target instructions, and cycling through the positions* (see column 18, lines 4-11, least significant four bits of a potential next decode program counter),

where after the second address indicator finished cycling through the positions (see column 18, line 19, 'as well as a carry bit'), *the first address indicator indicates the next storage position of the processing packet in the memory* (see column 18, lines 24-38, and FIG. 9A, the incrementer 762 that feeds the carry bit to the PC Latch (31:4)).

Christie's reference teaches the less significant four bits program counter (*second address indicator*) that provides least significant four bits of a potential next decode program counter to correspond to 4-bype ROP from program queue (see column 18, lines 4-11, least significant four bits of a potential next decode program counter), Christie uses (4:31) bits (*first address indicator*), named as more significant program counter to position to a byte boundary of a RISC instruction set or a X86 instruction. The less significant program counter, which provides least significant four bits of a potential next decode program counter, and the more significant program counter increment or branch to the next instruction within a ROP or queue of RISC or X86 according to the processor.

Christie discloses the less significant program counter of four bits corresponding to a four-byte ROP instruction. The number of processing target instructions in ROP, 4, is not power of 2.

However, the difference is only the exclusive number of implementation, where the number is conforming to standards in size in accordance to the length of a given instruction set.

Therefore, it would be obvious to an ordinary skill in the art when performing counting of an instruction set in which the length of the instruction set is not power of 2, would modify the counter in a **structural similarity**. Doing so would correspond to the number of instructions required by a given instruction set.

As per Claims 50-51: Claims 50 and 51 have the functionality corresponding to the Claim 49. Claims 50-51 are rejected in the same reason as set forth in connecting to the rejection of Claim 49.

As per claim 2:

-Regarding claim limitations of claim 2, Christie teaches further claim limitations "first program counter updating and second program counter updating" using the incrementer, adders, and multiplexers (see column 18, lines 4-23, and lines 24-38).

As per claim 3:

-Regarding claim limitations of claim 3, claim 3 is inherent from relative address values used in a program when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38) to perform adding that sets the address of the relative address value in the program counters. To perform the adding a relative value included in an instruction, Christie discloses that in a branch, an instruction is fetched and decoded. The counter identifies the next address of the target instruction, and uses adders, selectors, to form the next address (this mechanism is provided in the discussion column 18, lines 4-38).

As per claim 4:

-Regarding claim limitations of claim 4, claim 4 manipulates a calculation performed by adders in the first counter in the second counter. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 5:

-Regarding claim limitations of claim 5, claim 5 manipulates a calculation performed by adders in the first counter in the second counter corresponding to the functionality of claim 4. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 6:

-Regarding claim limitations of claim 6, claim 6 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in

'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 7:

-Regarding claim limitations of claim 7, claim 7 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 8:

-Regarding claim limitations of claim 8, claim 8 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 9:

-Regarding claim limitations of claim 9, claim 9 is inherent from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 10:

-Regarding claim limitations of claim 10, given the broadest interpretation of the claim in light of specification, Christie's processing packet is ROP which has a length number 4. Christie discloses the program counter (4:30) that is more significant than 4, the length of ROP.

As per claim 11:

-Regarding claim limitations of claim 11, functionality claim 11 is inherent in registers, read/write address buffers, cache, and fetch mechanism used to store data as shown in Christie's figures (Figures 1A...).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers:

(703) 872-9306 (for formal communication intended for entry);

(703) 746-5429 (for informal or draft communication, please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TED T. VO

TTV
Patent Examiner
AU 2122
July 9, 2004